ALPIDE

Introduction

* Alice Pixel Detector (ALPIDE) is a monolithic active pixel sensor (MAPS) based on TowerJazz 180nm CMOS technology.
* The sensor was created for the upgrade of the Inner Tracking System (ITS) of the ALICE experiment at CERN.
* Since 2012, several prototypes of the ALPIDE has been developed. []
* The final, optimized chip was validated in 2016 after substantial test-beam campaigns which show performance values beyond the requirements set by the ITS upgrade, listed in table ??. [G.Rinella 2016]
* The chip has a high detection efficiency (>99%), short deadtime (<10^-5 pixel^- event^-) and excellent spatial resolution (≈ 5um) for tracking charged particles. [

A screenshot of a cell phone

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[G.Rinella 2016]

Chip layout

* It measures 15 cm by 30 cm and contains more than five hundred thousand pixels, organized into 512 rows and 1024 columns??. [Abelev 2014 ?].
* Each pixel has a surface area 29.24 μm × 26.88 μm and a sensing diode (diameter ~2 um) who is approximately 100 times smaller than the pixel area.
* The peripheral region (1.2 x 30 mm2) implements analog biasing, control, readout and interfacing functionalities. [G. Rinella 2016]
* The chips is mostly made out of silicon (~40um thick) and is topped off with ~11um of aluminum.
* A 3D cut-out of the chip is presented in figure ??.
* The pixel matrix is grouped into 32 sections with 16 columns in each (16 col/sect x 32 sect = 512 col).
* During readout, sections are read out simultaneously and columns sequentially. Readout is controlled at the chip periphery.
* For every double column there is a dedicated priority encoder.
* Priority encoders are responsible for generating hit pixel address and sending said address to the periphery.(?)
* An illustration of the chip is presented in fig?? [pCT He Ions]

A screenshot of a computer

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Pixel

* A cross-sectional view of a pixel is illustrated in fig ??.
* The sensor is realized on a silicon substrate on which a highly resistive epitaxial layer (the active volume) is grown.
* Possible thickness of the active layer ranges from 18um to 30um.
* P-wells are placed into the epitaxial layer.
* A potential barrier forms where the heavily p-doped (P++) substrate and (P+) wells meet the lightly p-doped (P-) epitaxial layer.
* Electrons (e) are vertically confined by the potential barriers and diffuse laterally across pixels.

A close up of a map

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* The ALPIDE chip is based on the 180 nm CMOS technology of TowerJazz.
* An important design feature is the deep p-well which shields n-wells of pMOS transistor from the active layer.
* This prohibits diodes and n-wells from competing in collecting electrons.
* The feature allows the full use of CMOS circuitry in the epitaxial layer without impairing charge collection [S. Kushpil (2017)].
* The n-well diode, i.e. sensing element of the pixel, is surrounded by a depletion volume.
* Moderate reverse bias can be applied to the substrate in order to increase the depletion volume and improve charge collection. [S. Kushpil (2017)]
* The epitaxial layer is, for the most part, free of electric fields and charge is left to thermally diffuse in the active volume until it is collected by the diode or recombines with the atomic structure. Because of this, MAPS, in general, have slow collection times of approximately 100ns. [[\*](https://arxiv.org/pdf/1005.3710.pdf)]
* On top of the chip lay up to six aluminum metal layers suitable to implement high density and low digital circuits [Abelev 2014]. Does this include circuits other than in-pixel readout electronics?

A close up of a device

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**In-pixel front-end**

* Each pixel (28x28 um^2) embodies a collection diode and a front-end circuit. [G. Aglieri].
* ~~Each pixel has its own built-in readout circuit.~~
* The in-pixel circuit, as shown in fig??, comprise an input stage, an analog front-end and a digital front-end.

Analog front-end

* When hit by ionizing radiation, the active volume generates electron-hole pairs.
* The generated electron charge accumulates around the collection diode and induces a voltage signal in the input stage (fig.?? (a)).
* The continuous signal travels to analog front-end where it is shaped and amplified by an amplifier. The amplifier works as a delay line, with a peaking time of ~2us, and enables ALPIDE to be run in trigger mode.
* Also part of the analog front-end circuit is a comparator.
* The comparator has two analog inputs OUT\_A and THR and a digital binary output OUT\_D (0 or 1?).
* If the amplified signal OUT\_A exceeds a fix threshold voltage THR the comparator outputs a pulse OUT\_D. Period of the output is typically 5-10 us.

A close up of a map

Description automatically generated

Digital front-end

* The pulse continues to digital front-end where it encounters a STROBE signal.
* The STROBE signal provides a framing interval (a window) of a few nanometers.
* It is distributed globally to all pixels and can be activated either internally or externally.
* If the pulse from analog-front end coincides with a window hit information is latched on to one of the three in-pixel memory cells.
* These memory cells are in-pixels data storage elements also known by the collective term multi event buffer (MEB). MEB can store up to three hits simultaneously, one per buffer (i.e. memory cell).
* More/better ^

Mode of Operation

* Chip operation mode is determined by STROBE trigger settings.
* Continuous mode implements internal triggers while trigger mode relies on external provocation to generate a STROBE signal.
* When is what used?
* The ALPIDE chip is fabricated on a single slab of silicon and there are no physical boundaries separating pixels.
* Without such boundaries electrons diffuse freely between pixels.
* Particles with adequate ionizing energy are registered as hits.
* The ionizing radiation generates electrons in the active volume.
* The electrons diffuse in the active volume until they reach the depletion region where they drift are collected by the diode. The accumulation of electrons around the diode induce a voltage signal in the input stage of the in-pixel analog front-end circuit. The signal is sendt t
* The in-pixel circuitry first takes a continuous voltage signal and shapes it. If the shaped signal exceeds a fixed threshold voltage it is passed on to the digital section and stored in memory.

Fabrication

* Towerjazz 18nm CMOS technology is used to fabricate ALPIDE.
* The chip is realized on a heavily doped p-type substrate where a highly resistive epitaxial layer is grown. The epitaxial layer
* Readout electronics are integrated into the epitaxial layer.
* The technology also the deep p-well feature.
* Like the substrate, the p-well causes a potential barrier between itself and the epitaxial layer.
* While electrons generated in the pixel drift freely in the horizontal direction, they are vertically confined by the potential barriers.
* Another added benefit is the shielding of n-wells in the PMOS. This allows diodes to Without the p-well, n-wells and diodes compete in collection of electrons.
* The p-well also shields n-wells of PMOS transistors from electrons.

The chip is realized in a single slab of silicon. A

Pixel

* A pixel is a cubic volume of the chip in which all necessary pixel components, diode and readout electronics, are included.
* The diode is the signal sensing elements and has a diameter of ~2um (?), 100 times smaller than pixel cell area. [G. Rinella 2016]
* ALPIDE is fabricated using Towerjazz 18nm CMOS technology.
* A highly resistive epitaxial layer is grown on top of a heavily doped p-type substrate.
* Figure ?? illustrates a three-dimensional cut-out of ALPIDE.